IN THE SPECIFICATION

Please amend the portions of the Specification identified below to read as indicated herein.

Paragraph beginning at page 5, line 31:

Digital control interface 7 receives an address from microprocessor 3 and passes the address to array decoder logic 6. Array decoder logic 6 accesses a pixel in sensor array 105 based on the address. More specifically, array decoder logic ~~decoder~~ 6 converts the address into a row signal and a column signal that designate a position of a pixel in sensor array 105.

Paragraph beginning at page 6, line 5:

If necessary, digital control interface 7 reformats the address from microprocessor 3 for use by array decoder logic 6. For example, in the embodiment of RAIS 100 shown in FIG. 1, digital control interface 7 receives two 16-bit address words from microprocessor 3, and reformats the two 16-bit address words into a 32-bit address for array decoder logic 6. In this example, array decoder logic ~~decoder~~ 6 converts the 32-bit address into a row signal and a column signal that designate a position of a pixel in sensor array 105.

Paragraph beginning at page 11, line 20:

Single pixel access is handled by the direct addressing mode. Here the digital control interface 7 receives a y (row) and an x (column) address for a single pixel from microprocessor 3. Array decoder logic 6 applies the x and y components of the address to row decoder 4 and column decoder 5, respectively, for this address only, and only data from the single pixel that corresponds to the address is returned to microprocessor 3 through the digital control interface 7. This method is used to control readout or integration of single pixels.